

Jitter Measurements in High-Speed Serial Data Signals

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가 . '1', '0' 가
(jitter)가 가 .
,
Eye Diagram, Bathtub , TIE
.
PCI Express
.

I/O , LAN,

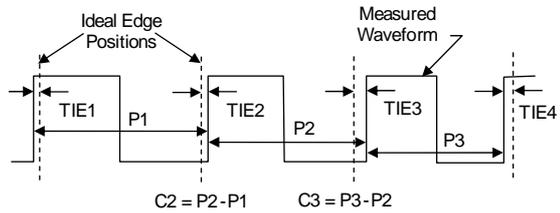
(differential signal)
LVDS
CDR
가 Infini-Band, PCI Express, 10Gigabit Ethernet, Fibre Channel, HyperTransport, RapidIO

[1].

가 BER
(budget) 10^{-12}
BER 4 3Gbps 가
Eye Diagram, Bathtub Plot, Histogram

1.

(reference point)
가
가
(1)
[2].



Period Jitter vs. Cycle-Cycle Jitter vs. Time Interval Error

(1)

• TIE:

- Period : (1) P1, P2, P3
- Cycle-Cycle : (1) C2, C3

3가

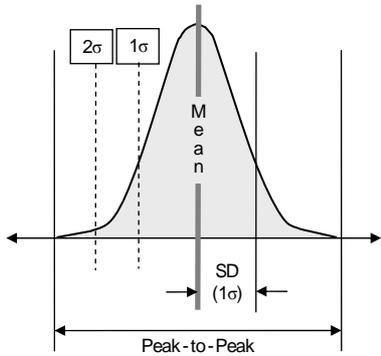
, crosstalk, impedance mismatch
가
Intersymbol Interference(ISI), duty-cycle distortion
thermal noise, pink noise

2.

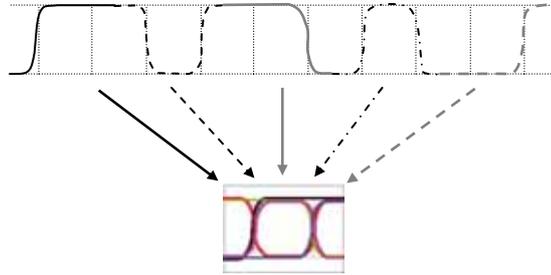
3가

“Bounded Jitter” “Deterministic Jitter”
“Unbounded Jitter”
“Random Jitter”
Unbounded Jitter Gaussian PDF
(total jitter) (phase error)
(1) deterministic
random

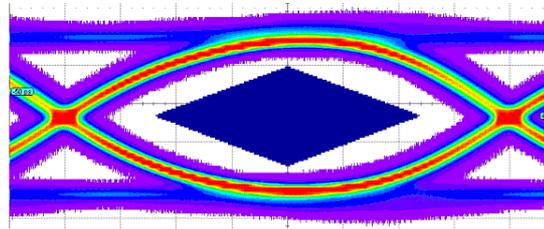
$$\varphi(t) = \varphi(t)_D + \varphi(t)_R \quad (1)$$



(2) Gaussian



(3) Eye Diagram



(4) Eye Diagram

Gaussian
 (2) Gaussian [3]
 가 (mean)
 TIE 0 . 1σ
 (standard deviation) Gaussian
 68.26% 가 4σ
 99.99366%
 10⁻¹²BER 7σ
 (2)
 (Jpp: Peak to Peak Jitter)[4].

$$J_{pp}^{Total} = J_{pp}^{Random} + J_{pp}^{Deterministic}$$

$$= 14σ + J_{pp}^{Deterministic} \quad (2)$$

3.

Histogram,
 Time Trend, Jitter Spectrum, Eye Diagram,
 Bathtub Curve

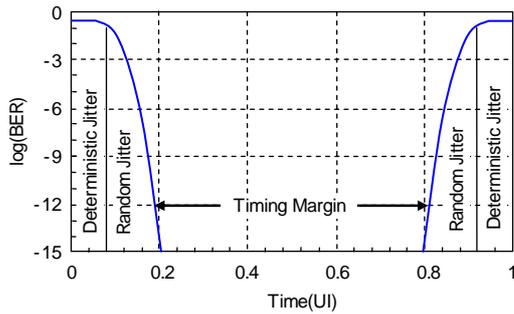
가. Eye Diagram

signal integrity
 eye diagram
 Eye diagram
 (amplitude) . Eye

diagram
 (3) 2UI
 eye diagram
 [2].
 (4) ()
 Eye diagram 가
 가 eye opening
 가 eye opening
 signal integrity가 eye opening
 . Bathtub Curve
 Gaussian
 eye diagram
 eye BER
 BER
 . Bathtub BER eye
 opening . Bathtub
 (BERT scan) (5) UI가 X

BER Y
 Deterministic
 random 가 BER
 가 가 가
 BER opening
 UI timing margin

TIE Histogram
 Histogram
 TIE histogram
 TIE histogram
 deterministic
 TIE histo-
 gram deterministic

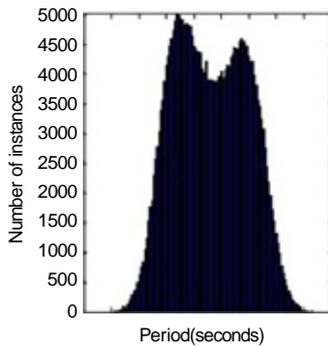


(6) TIE histogram [5].
 (6) (a), (b)
 deterministic
 , (c) deterministic

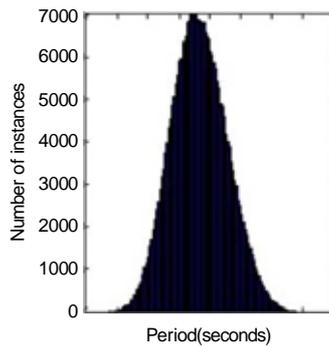
(5) Bathtub

Time Trend

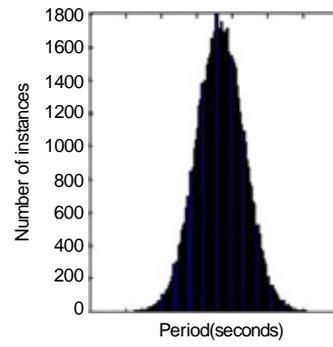
Jitter histogram



(a) TIE Histogram A

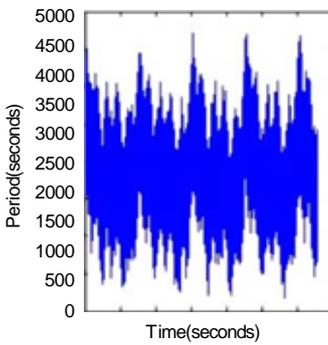


(b) TIE Histogram B

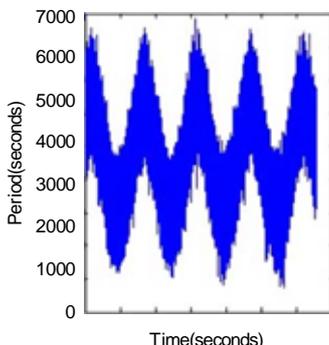


(c) TIE Histogram C

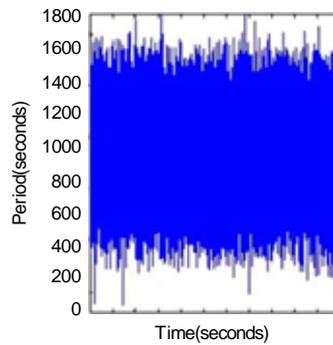
(6) TIE Histogram



(a) TIE Trend A



(b) TIE Trend B



(c) TIE Trend C

(7) Time Trend

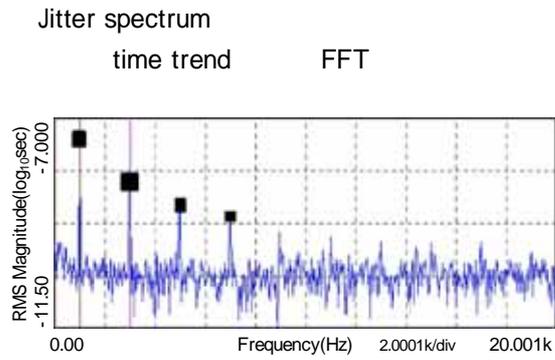


time trend
 . Time trend
 rise time, fall time, duty cycle, TIE
 . (7) (6) TIE histogram
 TIE time trend [5].
 (7) (a)
 , (b)
 . (c)
 TIE trend

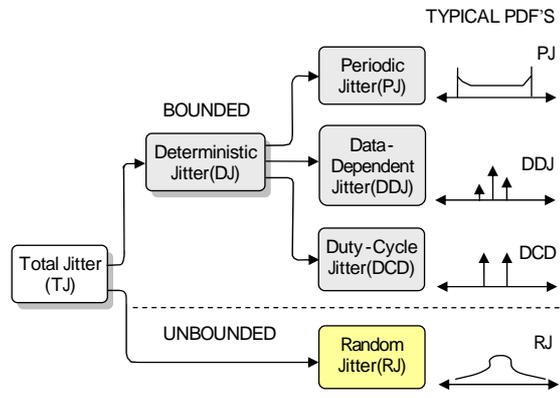
. (7a) 1kHz
 가 (8)[2] 1kHz
 ()
)
 4.

random jitter,
 deterministic jitter total
 jitter
 (9)

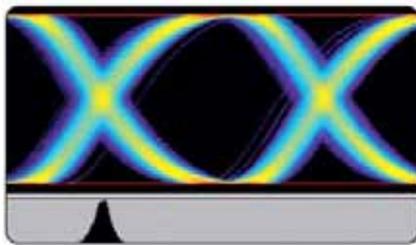
Jitter Spectrum



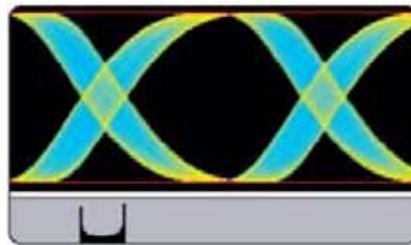
(8) Jitter Spectrum



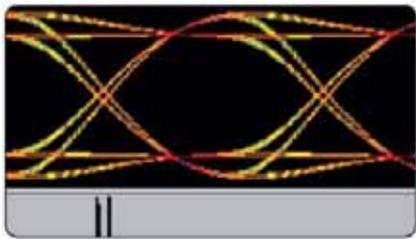
(9)



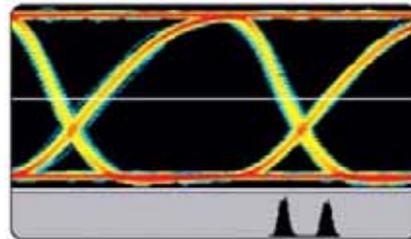
(a) Random Jitter



(b) Periodic Jitter



(c) Data-Dependent Jitter

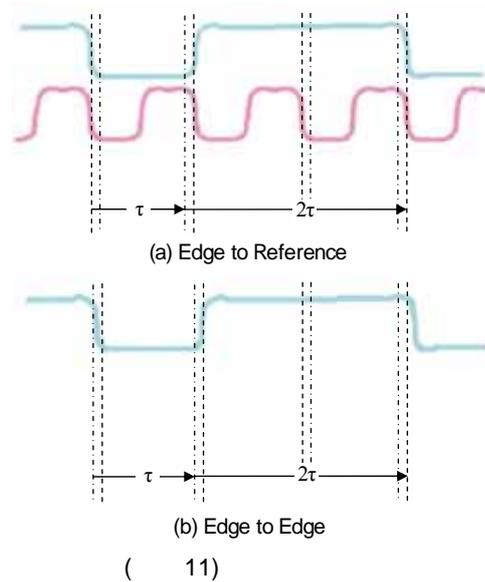


(d) Duty-Cycle Dependent Jitter

(10)

Eye Diagram TIE Histogram

(separation) [2]. TJ 가 DJ
 가 RJ .DJ SJ
 PJ DCD, ISI DDJ
 (10) RJ, PJ, DDJ, DCD eye dia-
 gram TIE histogram [2]. (
 10b) PJ RF
 TIE가
 Fourier series
 . (10c) DDJ ISI
 ISI impulse
 . (10d) DCD ,
 slew rate가
 decision threshold가



2.

BERT, RTSO, Sam-
 pling Oscilloscope, TIA가

1.

(measurement)
 edge to edge edge
 to reference
 Edge to edge
 edge to reference . (
 11a)
 (11b) edge to edge

가. RTSO

RTSO 가 eye
 diagram, histogram, data waveform, time trend,
 FFT (2005) 14GHz
 . 2004
 6GHz, 20GHz RTSO
 . NRZ
 1.8 [7].
 3.3Gbps
 (XAUI=3.125Gbps)

. BERT

BERT (threshold
 amplitude) 가

TIA

SerDes

가 tail fit
 RJ
 cycle plot DDJ
 cycle plot
 CDR
 가 PJ TIA
 BERT UI bathtub
 BER TJ = (BER) × RJ+DDJ+PJ [6].

3.

. Sampling Oscilloscope

가.

Sampling oscilloscope DCA 80GHz (12)
 , 200fs 가 , TDR (A), (B), (C),
 (Gbps) (D) [2].
 under -sampling (Tx) SMA
 RTSO (B) (A)
 (C) (D)

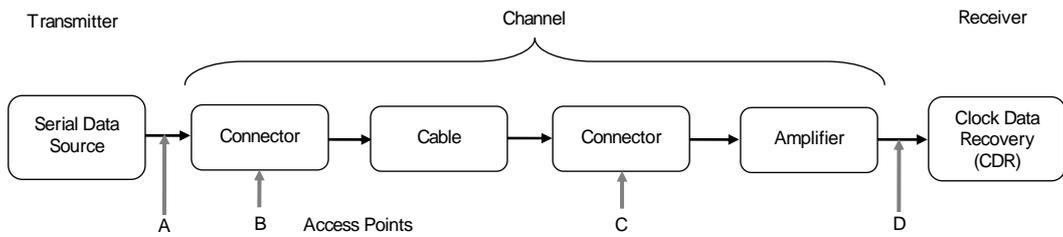
(Rx)
 (jitter tolerance) 가
 DDJ , TJ =
 (BER) × RJ+DDJ RJ
 , PJ 가 가 . (13) SerDes
 [6].

[8].

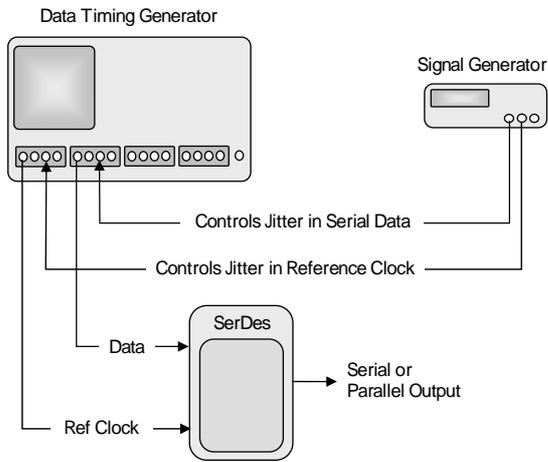
. TIA

(signal generator)
 (data timing generator)
 DUT SerDes

TIA



(12)



(13) SerDes

< 1>

	LeCroy SDA 6020 , BW=6GHz, Quad 20Gb/s Sampling
DUT	FPGA SerDes: RocketIO VertexII-Pro XC2VP30 FF1152-6
	Memec Design P160

< 2> RocketIO

	2.5Gbps PCI Express
Tx	Vod=1000mV, 10% Pre-emphasis 100ohm Termination Register
	ICS8422 LVDS 125MHz

< 1>

가 SerDes Xilinx FPGA
RocketIO
600Mb/s~3.125Gb/s
2.5Gbps
PCI express
(< 2>).
(14)



(14)

SMA

RTSO

가 ,
가 ,

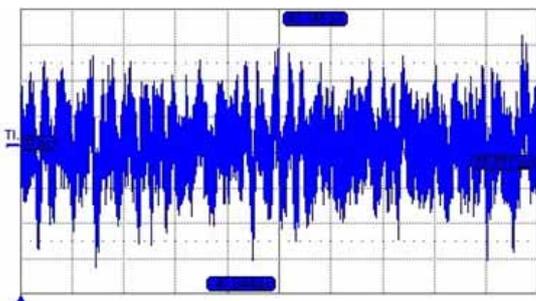
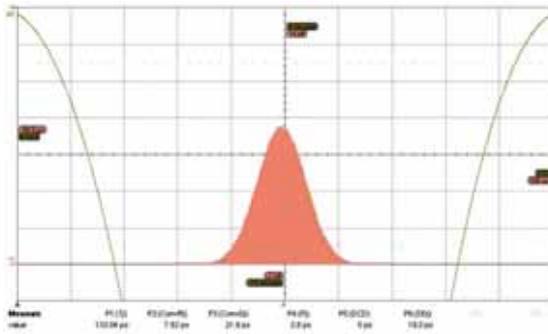
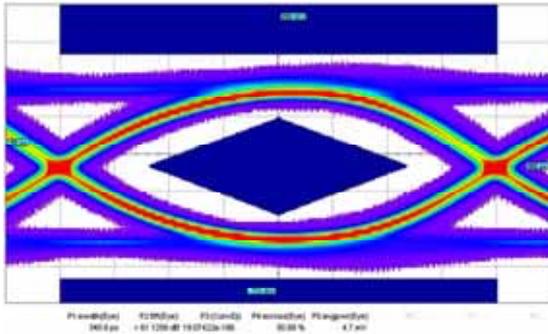
< 3>

(15), (16)
eye diagram, bathtub, TIE histogram, TIE trend
< 3>

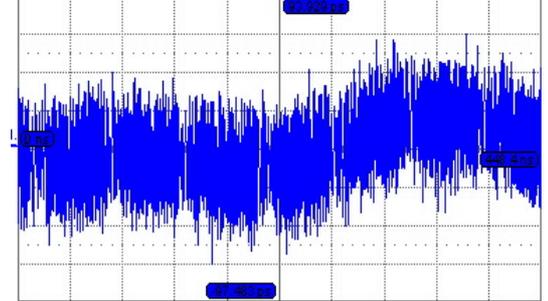
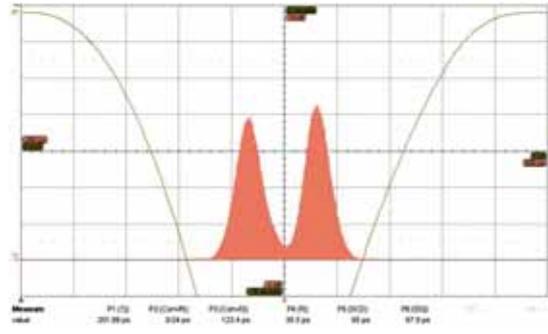
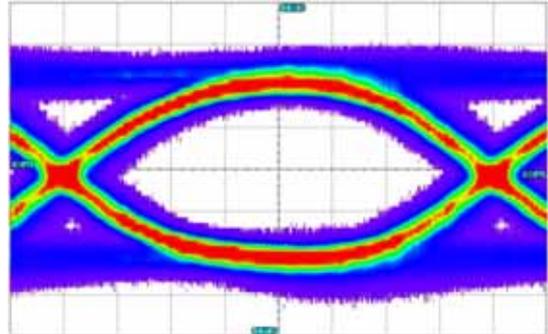
1 deterministic 21.9ps
0.05UI(1UI=400ps)

. De-

	(: ps)	
	1	2
RJ	7.82	9.04
DJ	21.9	123.4
PJ	2.8	35.5
DCD	5	65
DDJ	19	87.9
TJ	133.04	251.89



(15) (1)



(16) (2)

terministic ISI DDJ
 . TJ (2)
 133.04ps . , 10^{-12} BER
 0.67UI eye opening .
 Eye diagram PCI express
 (mask)가 eye
 . TIE histogram TIE
 trend 2 1
 1ps 가 . determinis-
 tic 123ps 1 5~6

가 가 . PJ, DCD, DDJ 가
 TJ 251.89ps 가
 . 2 10^{-12} BER 0.37UI eye
 opening . PCI express
 가
 . (16) eye diagram eye opening
 1 eye
 . TIE histogram (10) PJ
 DCD . TIE trend
 가 .

가
가

RTSO Real Time Sampling Oscilloscopes
 SJ Sinusoidal Jitter
 TDR Time Domain Reflectometry
 TIA Time Interval Analyzer
 TIE Time Interval Error
 UI Unit Interval

BER Bit Error Rate
 BERT Bit Error Rate Tester
 CDR Clock Data Recovery
 DCA Digital Communication Analyzer
 DUT Device Under Test
 FFT Fast Fourier Transform
 I/O Input/Output
 ISI Inter Symbol Interference
 LAN Local Area Network
 LVDS Low Voltage Differential Signaling
 NRZ Non-Return-to-Zero
 PDF Probability Density Function

[1] , , , “ , ” , 1110 , 2003. 8. 27., pp.16-24.
 [2] Understanding and Characterizing Timing Jitter, Tektronix, 2002.
 [3] Understanding Jitter, 2001 WAVECREST Corporation, 2001.
 [4] Jitter and the New Digital Regime, Brian Fetx, Agilent Technologies, 2003.
 [5] KT Tim cheng, D. Hong, CK Ong, and Li Wang, Jitter Extraction & Bit Error Rate Estimation for High Speed Serial Links, University of California, 2004.
 [6] ASDA-J , 2005 .
 [7] Jitter-Understanding It, Measuring It, Eliminating It, Johnnie Hancock, Agilent Technologies, 2004.
 [8] Jitter Generation Techniques for SerializerDeserialer Compliance Testing, Tektronix Application Note, 2005.